REMARKS

Claims 1-19 are currently pending in the subject application and are presently under consideration. A version of all pending claims is found on pages 2-6. Claims 3 and 5 have been amended herein to correct minor informalities. Favorable reconsideration of the subject patent application is respectfully requested in view of the comments and amendments herein.

I. Rejection of Claim 3 Under 35 U.S.C. §112

Claim 3 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is respectfully submitted that this rejection should be withdrawn for at least the following reason. Claim 3 is herein amended to cure such informalities and accordingly, withdrawal of this rejection is respectfully requested.

II. Rejection of Claims 1-19 Under 35 U.S.C. § 103(a)

Claims 1-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Schmidt *et al.*, U.S. Patent 5,212,631, in view of Sharma *et al.*, U.S. Patent 6,085,263. It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Neither Schmidt *et al.* nor Sharma *et al.*, alone or in combination, teach or suggest applicants' claimed invention, let alone there being no motivation to combine the references as suggested other than *via* employment of applicants' specification as a 20/20 hindsight-based road map to achieve the purported combination.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is established by a showing of three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) *must teach or suggest all the claim limitations.* *See* MPEP §706.02(j). The *teaching or suggestion to make the claimed combination* and the

> reasonable expectation of success *must be found in the prior art and not based on the Applicant's disclosure*. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). An examiner cannot establish obviousness by locating references which describe various aspects of a patent applicant's invention without also providing evidence of the motivating force which would impel one skilled in the art to do what the patent applicant has done. *Ex parte Levengod*, 28 USPQ2d 1300 (P.T.O.B.A.&I. 1993).

Independent claim 1 (and similarly independent claims 6, 9, 10 and 17) recites a system and/or method for an industrial controller with an I/O processor to optimize the exchange of shared data through the use of cache memory. This optimization is accomplished *via ~~an~~ **I/O processor both, storing input values in shared memory based upon forced I/O values stored in the cache memory, and determining output values based upon forced I/O values stored in the cache memory***. Thus, applicants' claimed invention provides for a novel system and/or method for utilizing cache memory. Neither Schmidt *et al.* or Sharma *et al.* (alone or in combination) teach or suggest such features of applicants' claimed invention.

In particular, Schmidt *et al.* is directed towards a programmable controller processor module comprising a ladder logic instruction processor, a communication processor, a general-purpose processor and an input/output module interface circuit coupled together by a common set of signal buses. Respective multiple sub-component processors accomplish specific specialized tasks rather than having a single unitary processor perform all the necessary functions. Thus, under Schmidt *et al.* the separation of the different logical functions from the unitary processor to specialized sub-module processors aids in reducing latencies inherent in the unitary scheme. The subject invention on the other hand, is directed primarily towards reducing access times to I/O force data for both the ladder processor and more particularly the I/O processor. In particular, the subject invention seeks to alleviate the latencies associated with conflicts that may arise when the I/O processor and ladder processor seek the same I/O force data simultaneously from the same memory address location. The subject invention accomplishes the reduction in latencies associated with access conflicts between the I/O processor and ladder processor through the use within the I/O processor of an ***operatively***

coupled cache memory storing at least a portion of the forced I/O values stored in shared memory, ensuring that the I/O processor both stores ***input values in the shared memory based at least in part upon forced I/O values stored in the cache memory***, as well as ***utilizing the forced I/O values stored in cache memory to determine output values***. As Examiner correctly points out, Schmidt *et al.* does not disclose such a facility. Consequently, Schmidt *et al.* neither teaches nor suggests all the limitations recited in the subject claims.

Sharma *et al.*, discloses an improved I/O processor for delivering high I/O throughput while maintaining inter-reference ordering among memory reference operations issued by an I/O device as specified by a consistency model in a shared memory multiprocessor system, e.g. a symmetric multiprocessor. In particular Sharma *et al.* employs a fully associative write-back cache (Sharma *et al.*, column 13, line 66); one where cache memory is written back to shared memory only upon a cache flush. The subject invention on the other hand, utilizes cache solely to store I/O force data that is downloaded from shared memory when: there is a cache fault, i.e. when currently valid force I/O data has not been loaded into cache because of constraints on the size of the cache; or when a message is received from the processor that a cache refresh has been initiated due to force I/O data being changed; or when force I/O data has been altered during program execution and a new set of force I/O data is to be loaded into cache from a particular memory address in the shared memory. Moreover, applicants' claimed invention not only uses the cache to store forced I/O data exclusively, but also bases its decisions on whether to store input values into shared memory in part on information stored in cache memory. Clearly then, Sharma *et al.* does not disclose a facility for the I/O processor to both, store input values in shared memory based in part upon forced I/O values stored in cache memory, as well as utilizing in part the forced I/O values stored in cache memory to determine output values.

Furthermore, given that Sharma *et al.*, on the one hand, addresses using two-way caching methodologies in reference to symmetric multiprocessing frameworks to enhance I/O throughput, and the subject invention, on the other hand, addresses the issue of using caching technology to overcome the problem of a plurality processors accessing the same time crucial data simultaneously in shared memory, there is no motivation for combining

Schmidt *et al.* and Sharma *et al.* to provide a blueprint for the subject invention. Any motivation or suggestion otherwise can only be sustained where applicants' specification is used as a 20/20 hindsight-based road map to achieve the purported combination. Thus, in view of the foregoing, it is respectfully requested that this rejection should be withdrawn.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

The Commissioner is authorized to charge the fee of $110.00 to Deposit Account No. 50-1063 (Order No. ALBRP226US) for the one month extension of time. In the event any other fees are due in connection with this matter, the Commissioner is authorized to charge Deposit Account No. 50-1063.

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

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